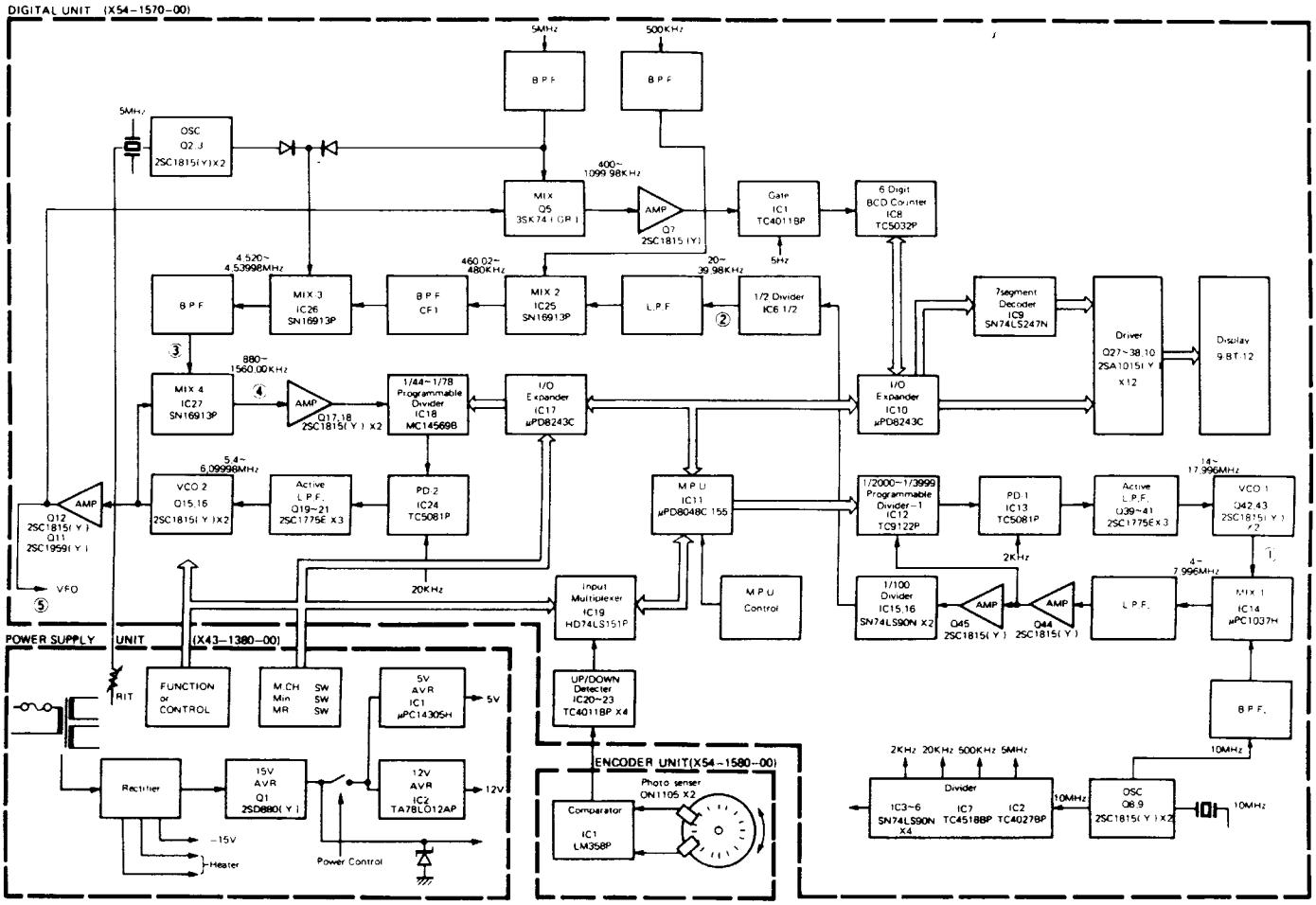


VFO-230 BLOCK DIAGRAM

Refer to Block Diagram

Display f. (kHz)	VFO f. (MHz) ⑤	IC12 14 Bit BCD data (1/M) M	Q42VCO f. (MHz) ①	IC6 (Pin 12) output f. (kHz) ②	IC27 (Pin 5) input f. (kHz) ③	IC18 7 Bit binary (1/N) N	B_3	B_2	B_1	A_4	A_3	A_2	A_1	IC27 output f. (kHz) ④
L 900.0	5.400.00	2 0 0 0	14.000	20.00	4520.00	44	0	1	0	1	1	0	0	880
L 900.0	5.400.02	2 0 0 2	14.004	20.02	4520.02	44	0	1	0	1	1	0	0	880
L 900.1	5.400.10	2 0 1 0	14.020	20.10	4520.10	44	0	1	0	1	1	0	0	880
L 900.8	5.401.60	2 0 8 0	14.160	20.80	4520.80	44	0	1	0	1	1	0	0	880
L 901.0	5.401.00	2 1 0 0	14.200	21.00	4521.00	44	0	1	0	1	1	0	0	880
L 909.9	5.409.98	2 9 9 8	15.896	29.98	4529.98	44	0	1	0	1	1	0	0	880
L 915.0	5.415.00	3 5 0 0	17.000	35.00	4535.00	44	0	1	0	1	1	0	0	880
L 919.9	5.419.98	3 9 9 8	17.996	39.98	4539.98	44	0	1	0	1	1	0	0	880
L 920.0	5.420.00	2 0 0 0	14.000	20.00	4520.00	45	0	1	0	1	1	0	1	900
L 950.0	5.450.00	3 0 0 0	16.000	30.00	4530.00	46	0	1	0	1	1	1	0	920
L 999.0	5.499.98	3 9 9 8	17.996	39.98	4539.98	48	0	1	1	0	0	0	0	960
0.0	5.500.00	2 0 0 0	14.000	20.00	4520.00	49	0	1	1	0	0	0	1	980
10.0	5.510.00	3 0 0 0	16.000	30.00	4530.00	49	0	1	1	0	0	0	1	980
100.0	5.600.00	2 0 0 0	14.000	20.00	4520.00	54	0	1	1	0	1	1	0	1080
200.0	5.700.00	2 0 0 0	14.000	20.00	4520.00	59	0	1	1	1	0	1	1	1180
300.0	5.800.00	2 0 0 0	14.000	20.00	4520.00	64	1	0	0	0	0	0	0	1280
400.0	5.900.00	2 0 0 0	14.000	20.00	4520.00	69	1	0	0	0	1	0	1	1380
500.0	6.000.00	2 0 0 0	14.000	20.00	4520.00	74	1	0	0	1	0	1	0	1480
599.9	6.099.98	3 9 9 8	17.996	39.98	4539.98	78	1	0	0	1	1	1	0	1560

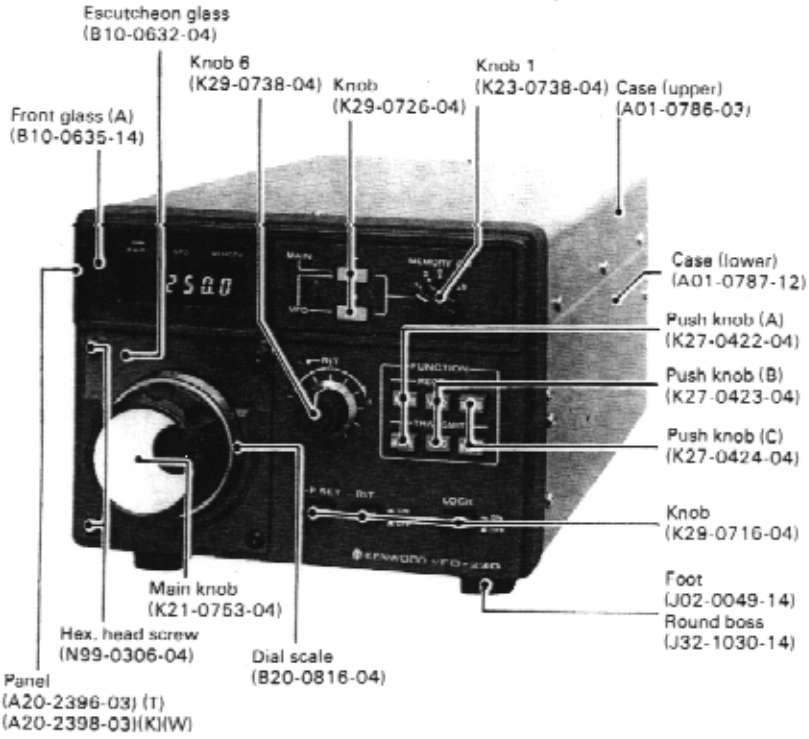
(Note) BAND: ○ ○ .0 MHz (ex. 14.0 MHz)

Table 13. Frequency chart

VFO-230

SPECIFICATIONS

Oscillation frequency	5.40 ~ 6.10 MHz	
Output voltage	0.2V ±3 dB	
Frequency stability	Within ±1 × 10⁻⁶ at 0 — 50°C	
	within ±3 × 10⁻⁶ at room temp.	
Power consumption	13W	
Power requirement	*AC 120V 50/60Hz (in U.S.A.)*	
	AC 220V/240V (Selectable) 50/60Hz (in Europe)	
Semiconductors used	CPU LSI	1
	FET	1
	IC	29
	Transistors	55
	Diodes	57
Dimensions	180 (182) W	7.09"
	133 (147) H	5.24"
	287 (330) D mm	11.30"
	(Figures in ( ) include projections.)	
Weight	Approx. 3 kg (6.61 Lbs.)	



CIRCUIT CONFIGURATION

The VFO-230 consists of a double PLL loop: the 1st loop covering a 20 kHz bandwidth at 20 Hz step, and the 2nd loop covering a 700 kHz bandwidth at 20 kHz step.

As the tuning dial is turned, an optical encoder (using a photo sensor) converts the dial rotation and its direction of rotation into an electrical signal, which is coupled to microprocessor IC11 (μPD8048C-155).

The microprocessor internally processes this dial signal and outputs the processed result as frequency-division data for the PLL and, at the same time, provides the corresponding dial display data.

In the 1st PLL loop, MIXER-1 (IC14: μPC1037H) combines the output of VCO-1 (Q42, 43) at 14~17.998 MHz with a 10 MHz reference frequency to convert the output to 4.0~7.996 MHz. This output is amplified and coupled to Programmable Divider 1 (IC12), where it is frequency-divided according to the division data from the microprocessor into a 2 kHz signal.

The phase of this 2 kHz signal is compared with that of the reference 2 kHz signal by phase comparator PD-1 (IC13), and this output is fed back to control the output frequency of VCO-1.

The 4~7.998 MHz signal (at 4 kHz steps) generated in the 1st PLL loop is further frequency-divided by a 1/100 (IC15, 16) and 1/2 (IC6 1/2) divider into a 20~39.98 kHz signal (at a 20 Hz step). This signal is coupled to MIXER-2 (IC25), where it is mixed with a reference 500 kHz signal which converts the signal to 480~460.02 kHz. The output of the second mixer goes through a narrow band ceramic filter (CF1), then couples to a third mixer, MIX-3 (IC27), where it is further mixed with a 5 MHz signal. The signal is now converted to 4520~4539.98 kHz. A reference 5 MHz signal is usually used for the other input of this third mixer. However, it is supplied from the crystal oscillator (Q2) for RIT operation or CW transmission. When the RIT feature is ON, the voltage applied across the varicap diode in the crystal oscillator is varied by the RIT control to obtain a frequency variation range of ±900 Hz. During CW transmission, the voltage across the varicap diode is adjusted by variable resistor VR1 on the digital unit to provide this oscillator with an output frequency 800 Hz higher than its original frequency. The output of MIX-3 goes through a band-pass filter (T2, T3, T4), and then couples to a fourth mixer, MIX-4 (IC26). Here it is mixed with the output of VCO-2 (5.4~6.09998 MHz) and is converted to 880~1560 kHz. This output, after amplification, is coupled to Programmable Divider 2 where it is frequency-divided to an output frequency of 20 kHz according to the division data supplied from the microprocessor. This output goes to phase detector PD-2 (IC24), where its phase is compared with the 20 kHz reference signal to create the frequency control signal for VCO-2.

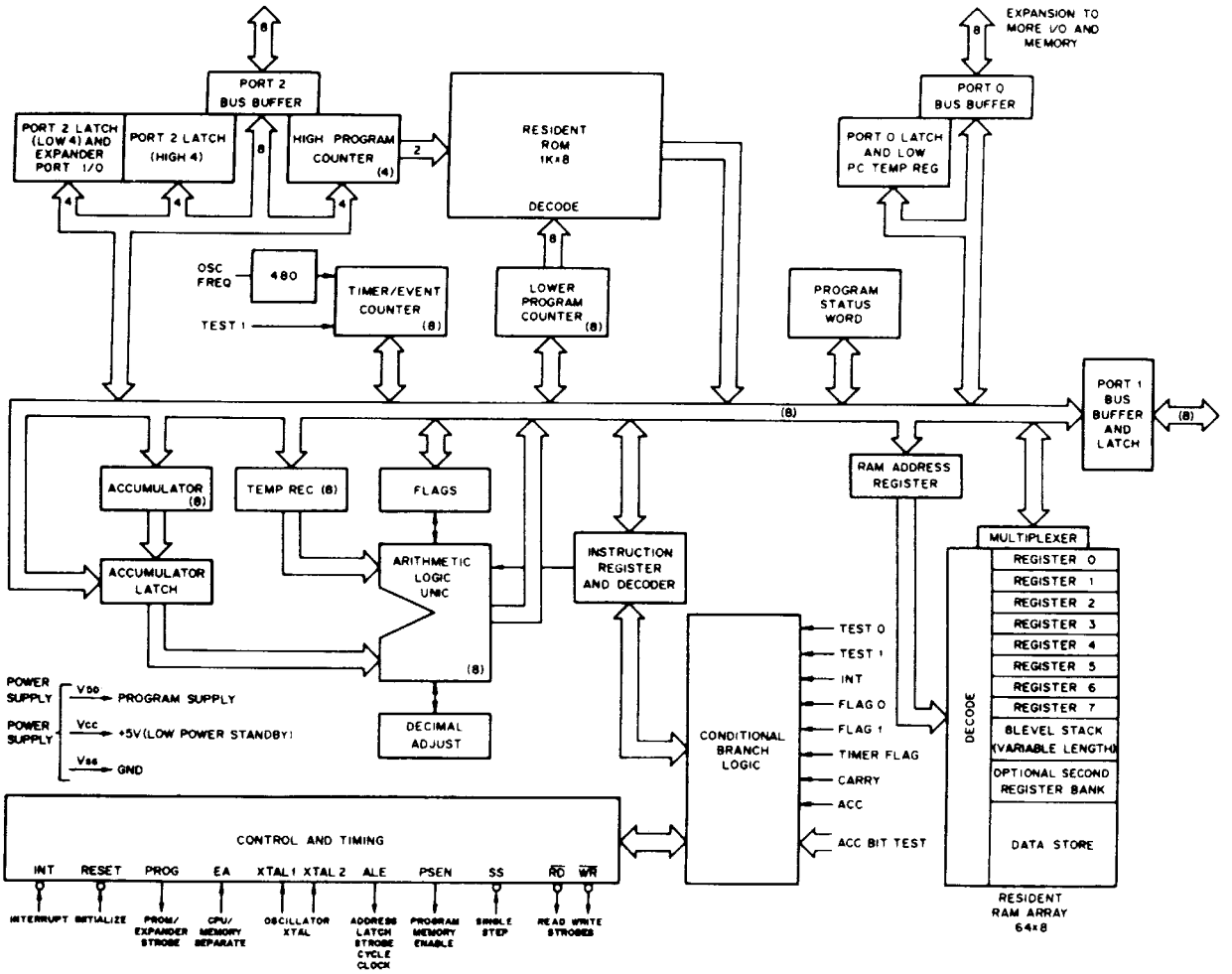
All the circuits hitherto described are always operating. However, the digital VFO provides its output intermittently to control the buffer amplifier. When the VFO in the main unit is operating, this VFO output is mixed with a 5 MHz reference signal by MIX 5 (Q5), of which output at 400 kHz to 1099.98 kHz is amplified, then counted up by a 6-digit frequency counter (IC8). The output data of this counter is stored into the microprocessor's memory.

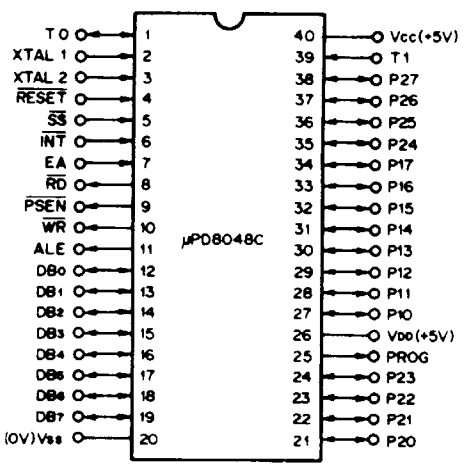
As seen above, all frequencies except the RIT and CW transmission shift frequencies are composed of combinations of reference frequencies. As a result, the accuracy and stability of the digital VFO output frequency is identical to that of the 10 MHz reference oscillator.

The frequency display resolution is identical to that of the main unit (down to 100 Hz) except for the RIT and CW transmission frequency display. This is accomplished by dynamically driving the fluorescent display tube based on the display and column data furnished by the microprocessor. The power to the VFO-230 is interlocked with that of the main unit. If, however, the VFO-230 is plugged into an AC outlet, the display, memory and output of the VFO remain live even when the power switch on the main unit is OFF. Therefore, when the main unit is again powered-on, the operating state set prior to power-off will reappear. Back-up power consumption for the VFO-230 is approximately 10 mA at 5V.

Item	Rating
Center frequency	470 kHz
6 dB bandwidth	±12.5 kHz or more
50 dB bandwidth	±25 kHz or less
Ripple (within 455±8 kHz)	3 dB or less
Loss	4 dB or less
Guaranteed attenuation	35 dB or less within 455±100 kHz
Input and output impedance	1.5 kΩ

Fig. 11 Ceramic filter (L71-0321-05) CFW470C (DIGITAL UNIT, CF 1)





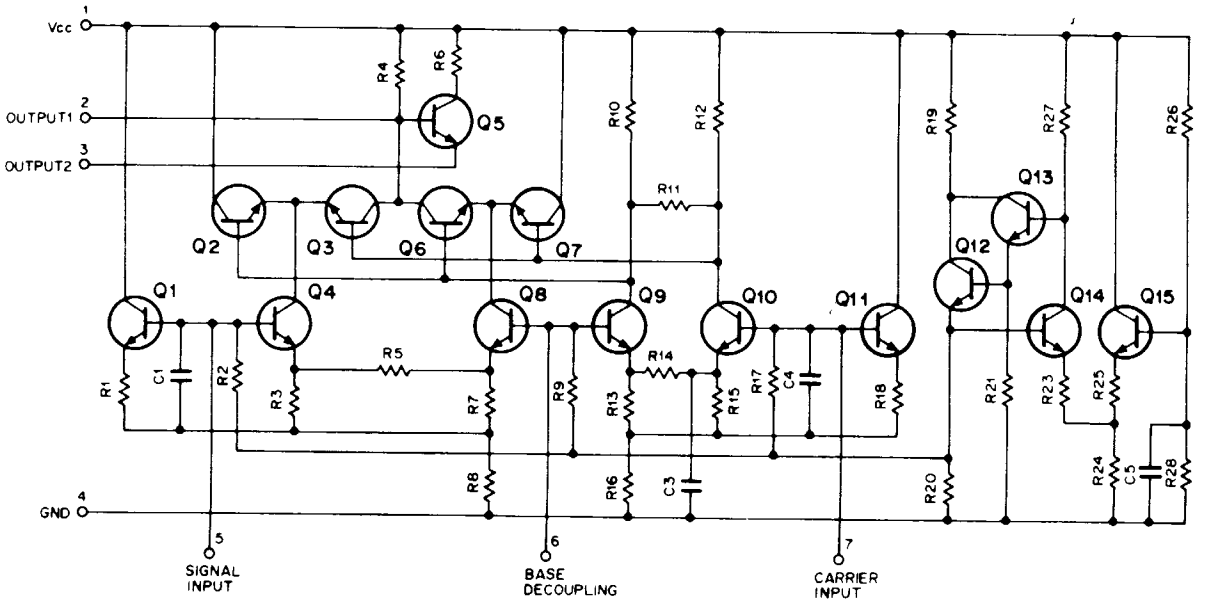
Terminals

P10 ~ P17	Input and output port (PORT 1)
P20 ~ P27	Input and output port (PORT 2)
$DB_0 \sim DB_7$	Data bus
T0, T1	Test
$\overline{INT}$	Interrupt
$\overline{RD}$	Read
$\overline{WR}$	Write
ALE	Address latch enable
$\overline{PSEN}$	Program store enable
$\overline{RESET}$	Reset
$\overline{SS}$	Single step
EA	External access
XTAL 1, 2	Crystal input

Maximum rating (Ta = 25°C)

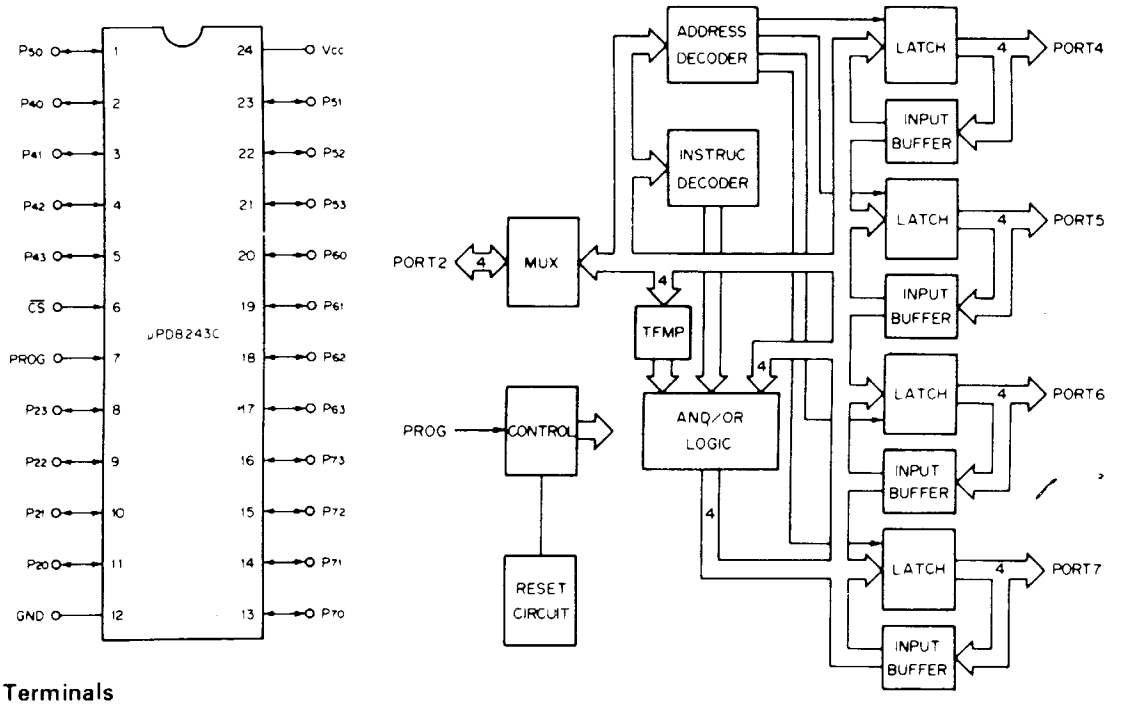
Item	Symbol	Rating
Operating voltage	Vcc	−0.5 ~ +7.0V
	VDD	−0.5 ~ +7.0V
Input voltage	Vi	−0.5 ~ +7.0V
Output voltage	Vo	−0.5 ~ +7.0V
Operating temperature	Topt	0 ~ +70°C
Storage temperature	Tstg	−65 ~ +150°C

Fig. 13 μPD8048C-155 (DIGITAL UNIT, IC11)



Item	Symbol	Rating
Operating voltage	Vcc	9.0V
Dissipation	Pd	270 mW (Ta = 75°C)
Operating temperature	Topt	−30 ~ +75°C
Storage temperature	Tstg	−40 ~ +125°C

Fig. 14 μPC1037H Double Balanced Modulator (DIGITAL UNIT, IC14)



Terminals

$P_{20} \sim P_{23}$	Input Output (Port 2)
$P_{40} \sim P_{43}$	Input Output port (Port 4)
$P_{50} \sim P_{53}$	Input Output port (Port 5)
$P_{60} \sim P_{63}$	Input Output port (Port 6)
$P_{70} \sim P_{73}$	Input Output port (Port 7)
$\overline{CS}$	Chip Select
PROG	Program pulse
	Input Output port (Port 2)

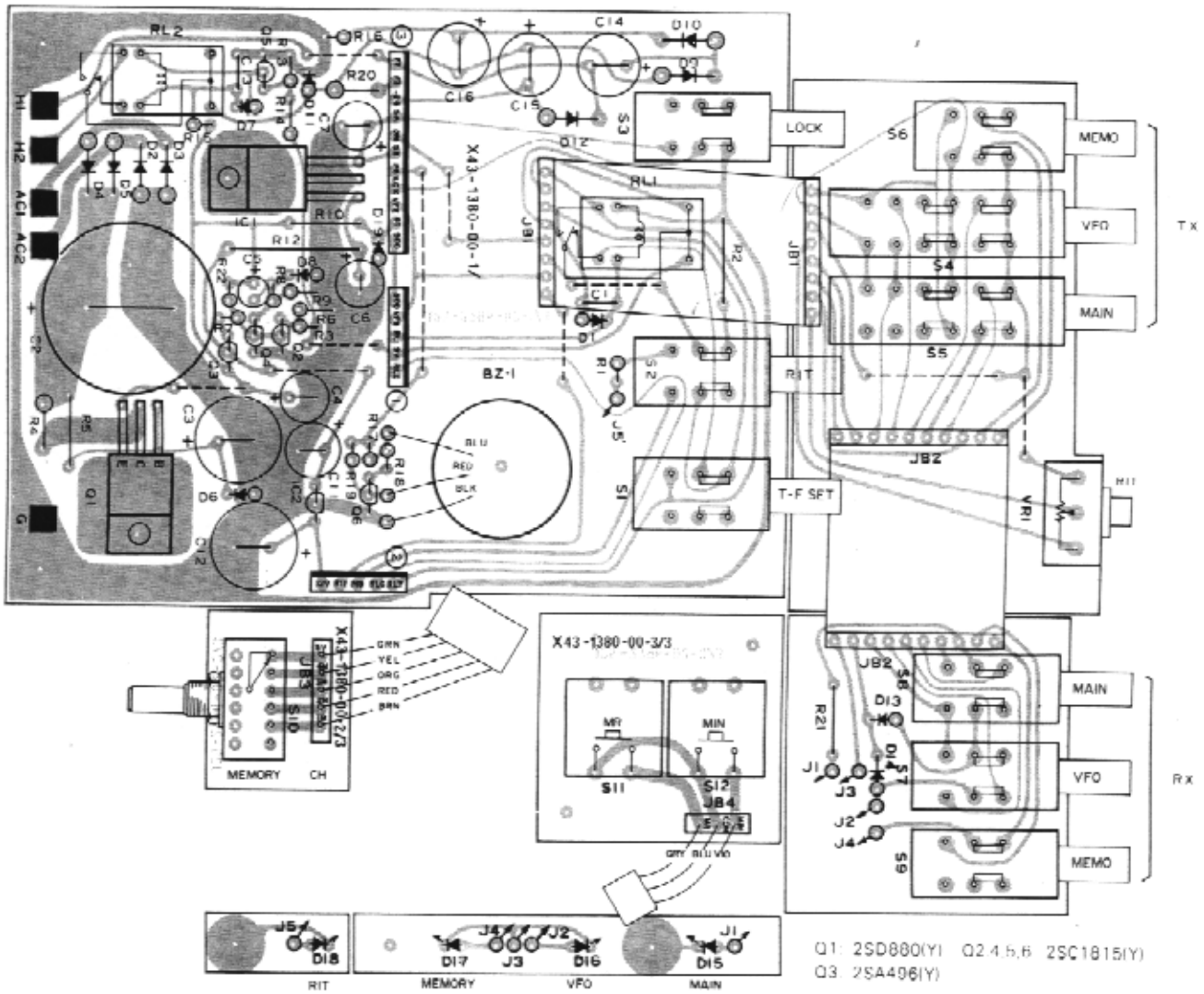
Maximum Rating (Ta = 25°C)

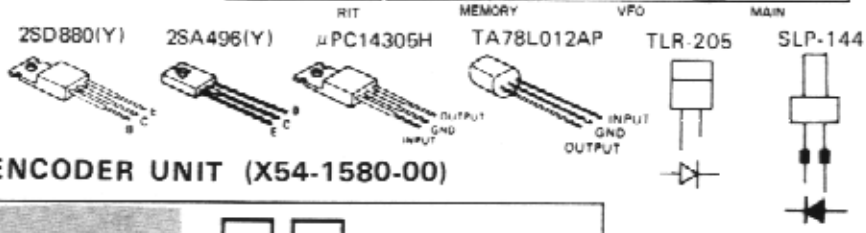
Item	Symbol	Rating
Operating voltage	Vcc	−0.5 ~ +7V
Input voltage	Vi	−0.5 ~ +7V
Output voltage	Vo	−0.5 ~ +7V
Operating temperature	Topt	0 ~ +70°C
Storage temperature	Tstg	−60 ~ +150°C

Fig. 15 μPD8243C (DIGITAL UNIT, IC10, 17)

VFO-230

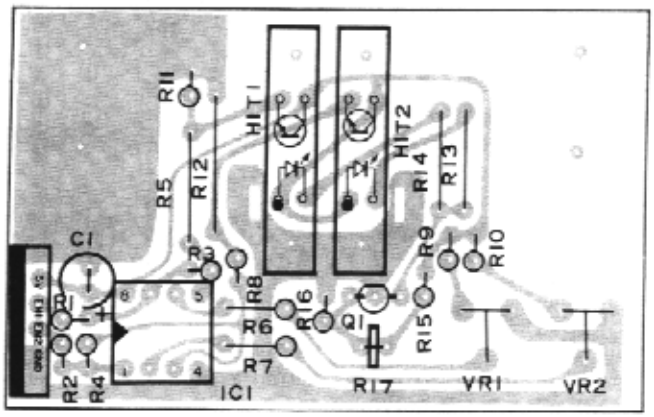
▼ POWER SUPPLY UNIT (X43-1380-00)



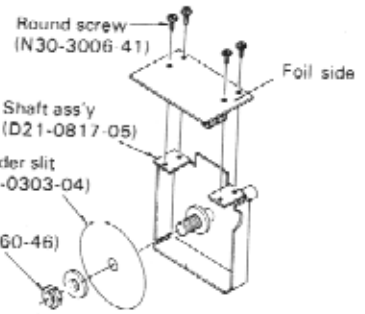


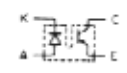
Q1: 2SD880(Y) Q2,4,5,6: 2SC1815(Y)
Q3: 2SA496(Y)
IC1: μPC14305H IC2: TA78L012AP
D1,7,8,13,14: 1S1555 D2~5,9,10,12: V06B
D6: WZ-150 D19: XZ-049 D15~17: TLR205
D18: SLP-144

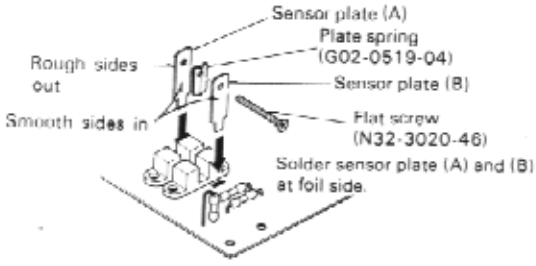
▼ ENCODER UNIT (X54-1580-00)



Q1: 2SA1015(Y)
IC1: LM358P
HIT1,2: ON1105







Max. Rating

VR	IF	PD	IC	V+ max	V- max	PC	Topr
3V	50mA	75mW	20mA	30V	5V	100mW	-25 ~ +85°